IDS 04/29/02

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JC13 Rec'd PCT/PTO 28 FEB 2002
Sheet 1 of 1

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-311US1	Application No.
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 28, 2002	Group Art Unit

U.S. Patent Documents

Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
W	AA	5,812,839	09/22/1998	Hoyt et al.			
W	AB	6,009,515	12/28/1999	Steele, Jr.			
W	AC	6,076,158	06/13/2000	Sites et al.			
W	AD	6,079,014	06/20/2000	Papworth et al.			
W	AE	6,115,811	09/05/2000	Steele, Jr.			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
W	AQ	Chang et al., "Branch Classification: a New Mechanism fro Improving Branch Predictor Performance", ACM 1994, pgs 22 - 31
	AR	
	AS	
	AT	

Examiner Signature	Date Considered

EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Substitute Disclosure Form (PTO-1449)

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IDS 06/09/04

Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-311US1	Application No. 10/070,008
Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))		Applicant Gilbert Wolrich et al.	
		Filing Date February 28, 2002	Group Art Unit 2183

Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation Yes	Translation No
	AA	WO 01/50679	07/12/2001	WIPO				
	AB	WO 01/50247	07/12/2001	WIPO				
	AC	WO 01/48619	07/05/2001	WIPO				
	AD	WO 01/48606	07/05/2001	WIPO				
	AE	WO 01/48599	07/05/2001	WIPO				
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	AP	EP 0 745 933	12/04/1996	Europe				
	AQ	EP 0 633 678	01/11/1995	Europe				
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	AU	Agarneal et al., "April: A Processor Architecture for Multiprocessing," Proceedings of the 17th Annual International Symposium on Computer Architecutre, IEEE, pp. 104-114.
	AV	Byrd et al., "Multithread Processor Architectures," *IEEE Spectrum*, Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
	AW	Chang et al., "A New Mechanism For Improving Branch Predictor Performance," IEEE, pp. 22-31 (1994).

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(37 CFR §1.98(b))		Filing Date February 28, 2002	Group Art Unit

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AX	Doyle et al., *Microsoft Press Computer Dictionary*, 2nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.
	AY	Farkas et al., "The multicluster architecture: reducing cycle time through partitioning," IEEE, vol. 30, December 1997, pp. 149-159.
	AZ	Fillo et al., "The M-Machine Multicomputer," IEEE Proceedings of MICRO-28, 1995, pp. 146-156.
	AAA	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," *Journal of Parallel and Distributed Computing*, Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117.
	ABB	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998.
	ACC	Hauser et al., "Garp: a MIPS processor with a reconfigurable coprocessor," Proceedings of the 5th Annual 1EEE Symposium on Field-Programmable Custom Computing Machines, 1997.
	ADD	Hennessy et al., "Complete Organization and Design: The Hardware/Software Interface," Morgan Kaufman Publishers, 1998, pp. 476-482.
	AEE	Hyde, R., "Overview of Memory Management," *Byte*, vol. 13, no. 4, 1998, pp. 219-225.
	AFF	Intel, "1A-64 Application Developer's Architecture Guide," Rev.1.0, May 1999, pp. 2-2, 4-29 to 4-31, 7-116 to 7-118 and c-21.
	AGG	Keckler et al., "Exploiting fine grain thread level parallelism on the MIT multi-ALU processor," IEEE, June 1998.
	AHH	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55.
	AII	Mendelson et al., "Design Alternatives of Multithreaded Architecture," *International Journal of Parallel Programming*, vol. 27, no. 3,Plenum Press, New York, USA, June 1999, pp. 161-193.
	AJJ	Schmidt et al., "The Performance of Alternative Threading Architectures for Parallel Communication Subsystems," Internet Document, *Online!*, 13 November 1998.
	AKK	Thistle et al., "A Processor Architecture for Horizon," IEEE, 1998, pp. 35-41.
	ALL	Tremblay et al., "A Three Dimensional Register File for Superscalar Processors," IEEE Proceedings of the 28th Annual Hawaii International Conference on System Sciences, 1995, pp. 191-201.
	AMM	Trimberger et al, "A time-multiplexed FPGA," Proceedings of the 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines," 1998.
	ANN	Turner et al., "Design of a High Performance Active Router," Internet Document, *Online*, 18 March 1999.
	AOO	Vibhatavanijt et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359.
	APP	Wadler, "The Concatenate Vanishes," University of Glasgow, December 1987 (revised November 1989), pp. 1-7.
	AQQ	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993.

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	10/27/04

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